

FIG. 1 (PRIOR ART)

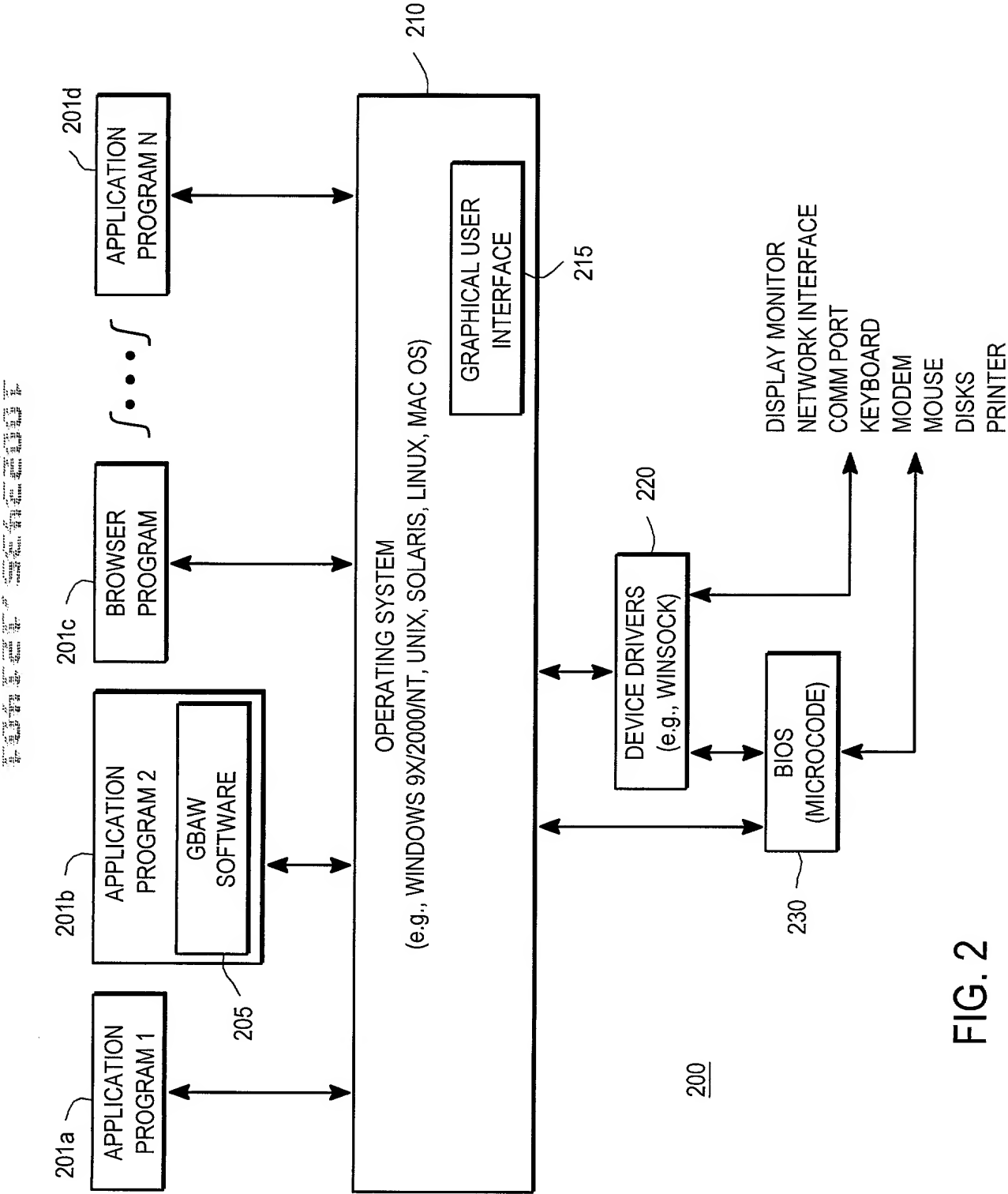


FIG. 2

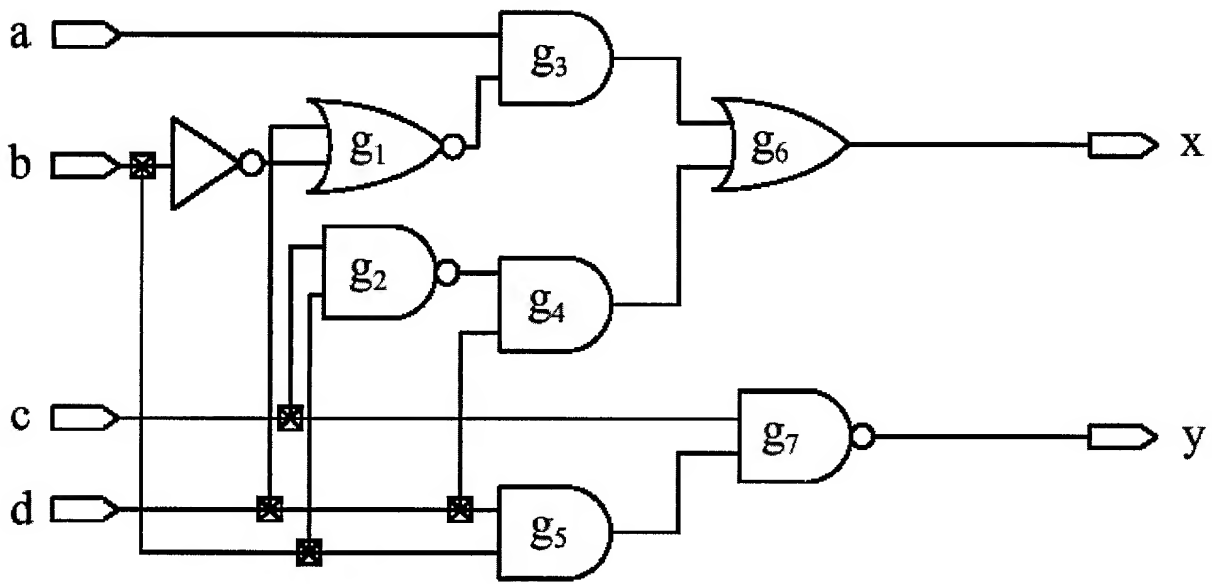


FIG. 3A

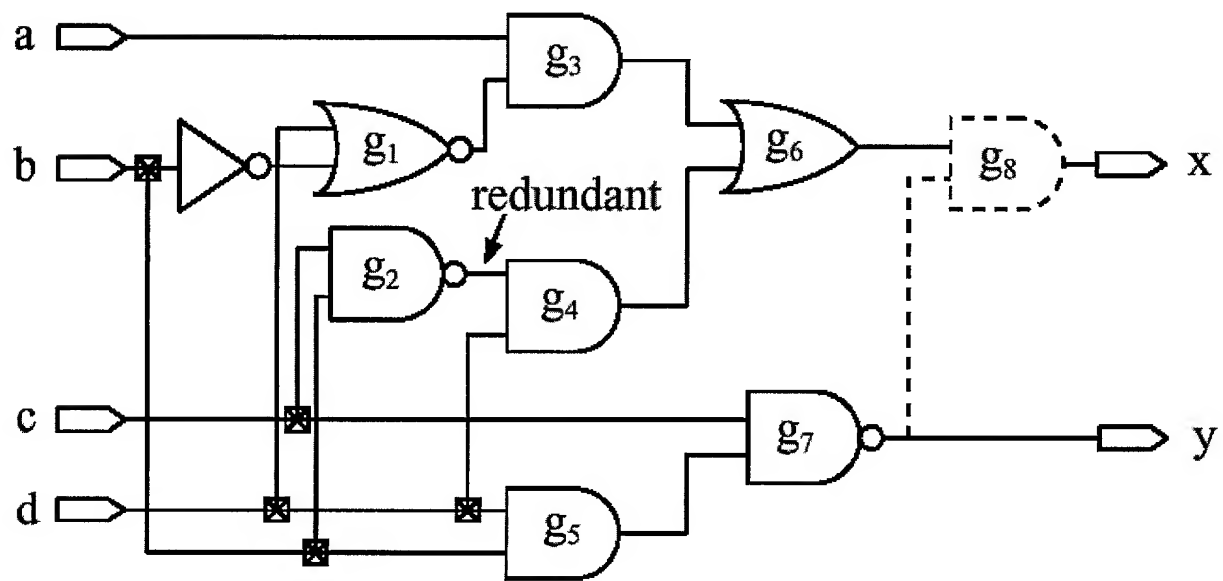


FIG. 3B

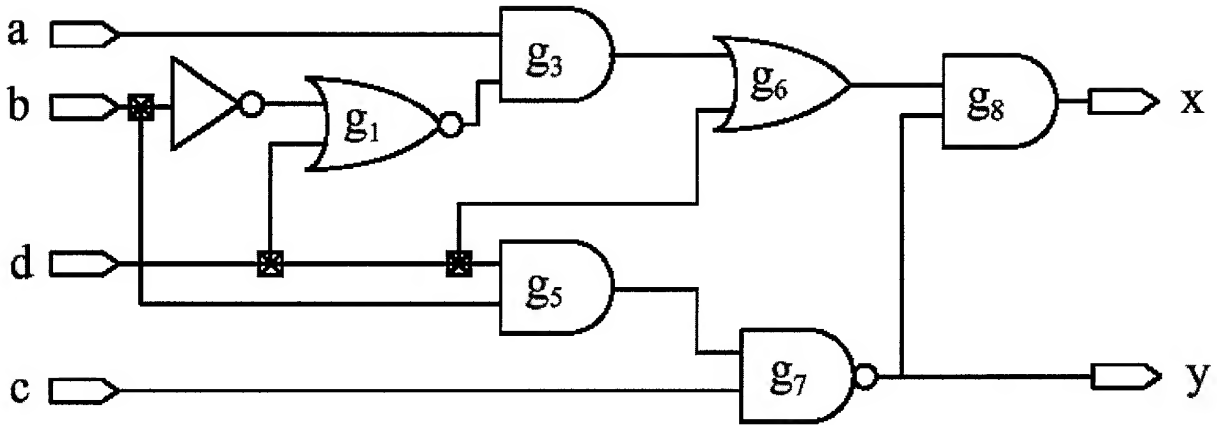


FIG. 3C

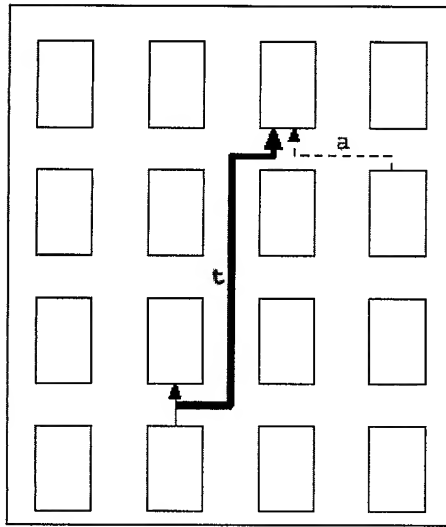


FIG. 3D

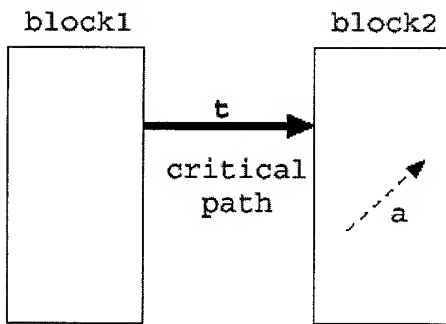


FIG. 3E

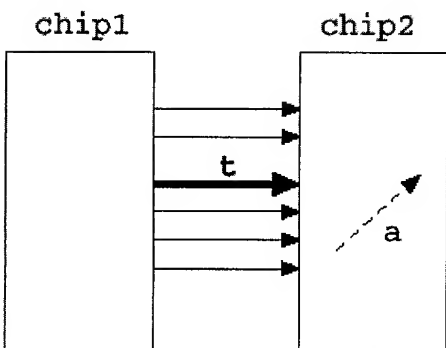


FIG. 3F

1. The present invention relates to a method for determining a critical path in a circuit. The method includes: (a) determining a set of blocks in the circuit; (b) determining a set of paths in the circuit; (c) determining a critical path in the circuit; and (d) determining a delay time for the critical path.

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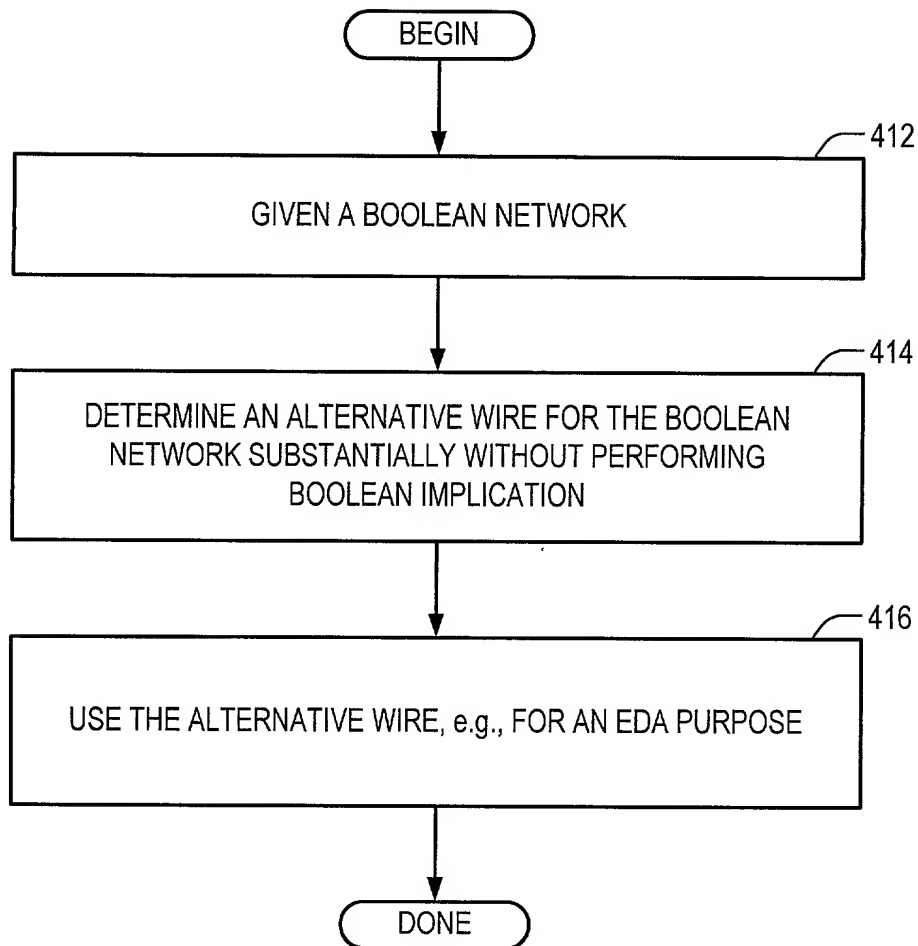


FIG. 4

510

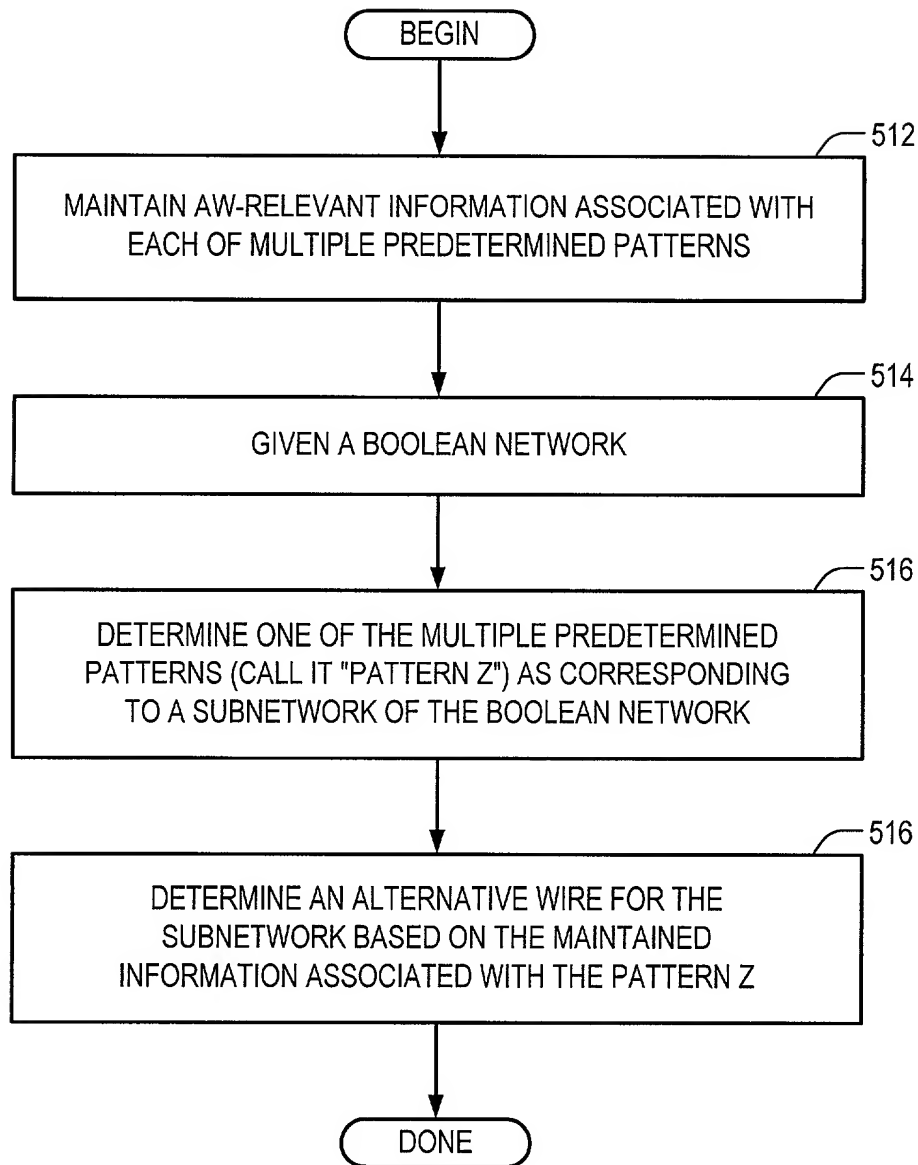


FIG. 5

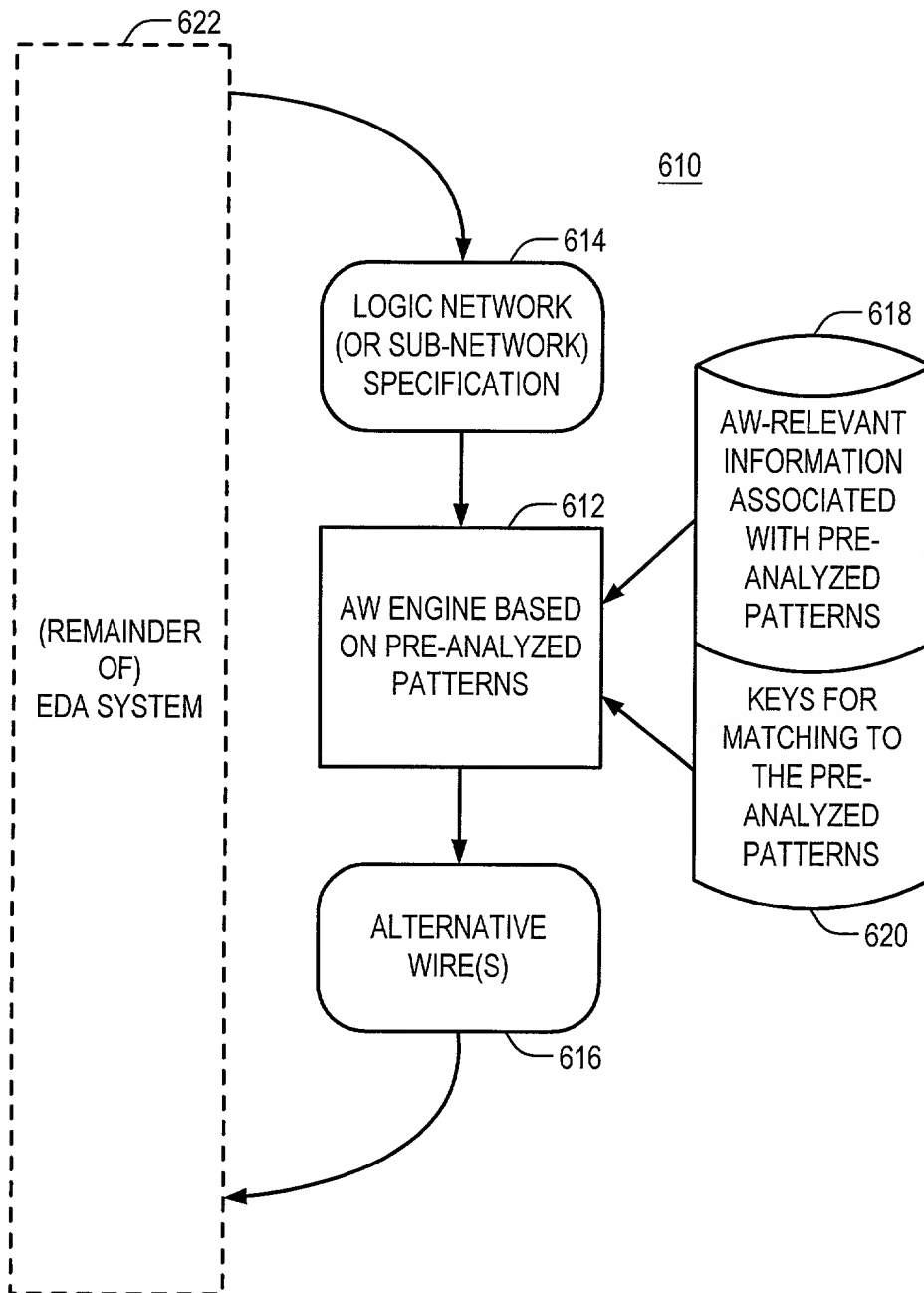


FIG. 6

710

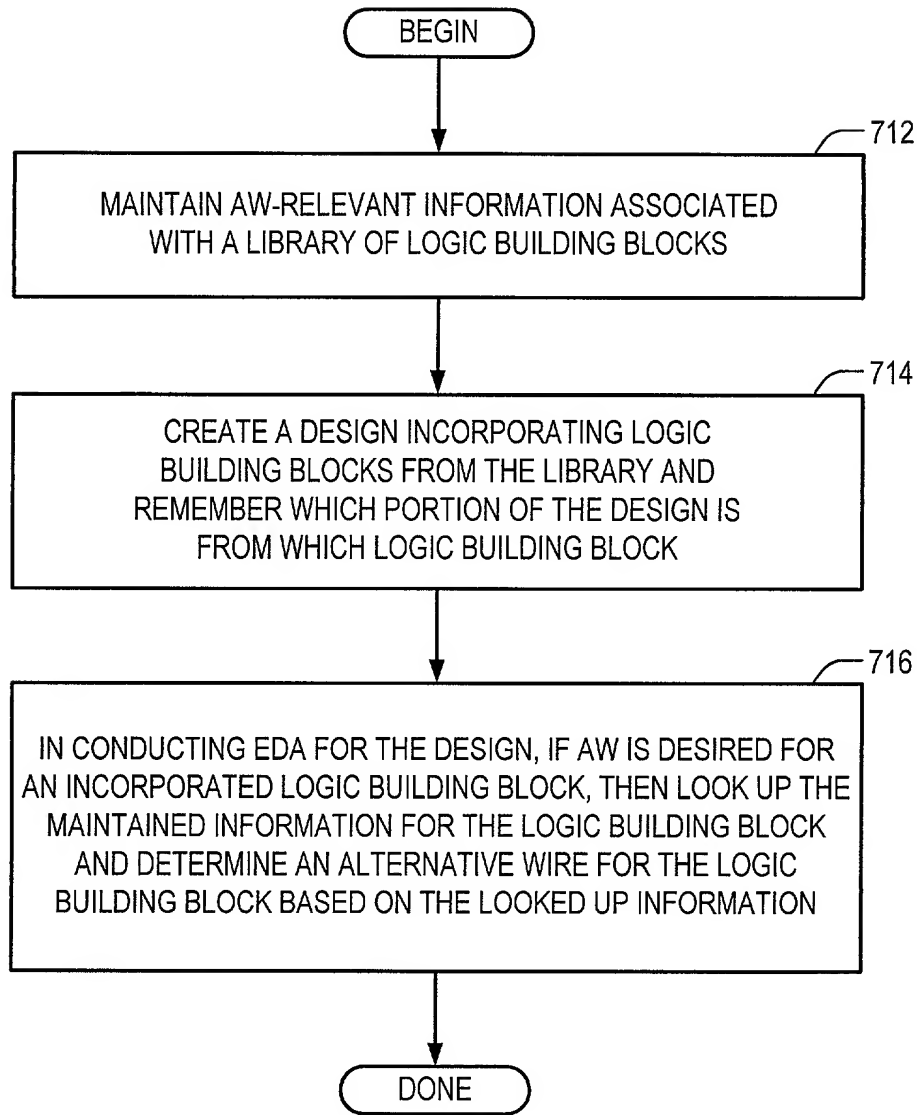


FIG. 7

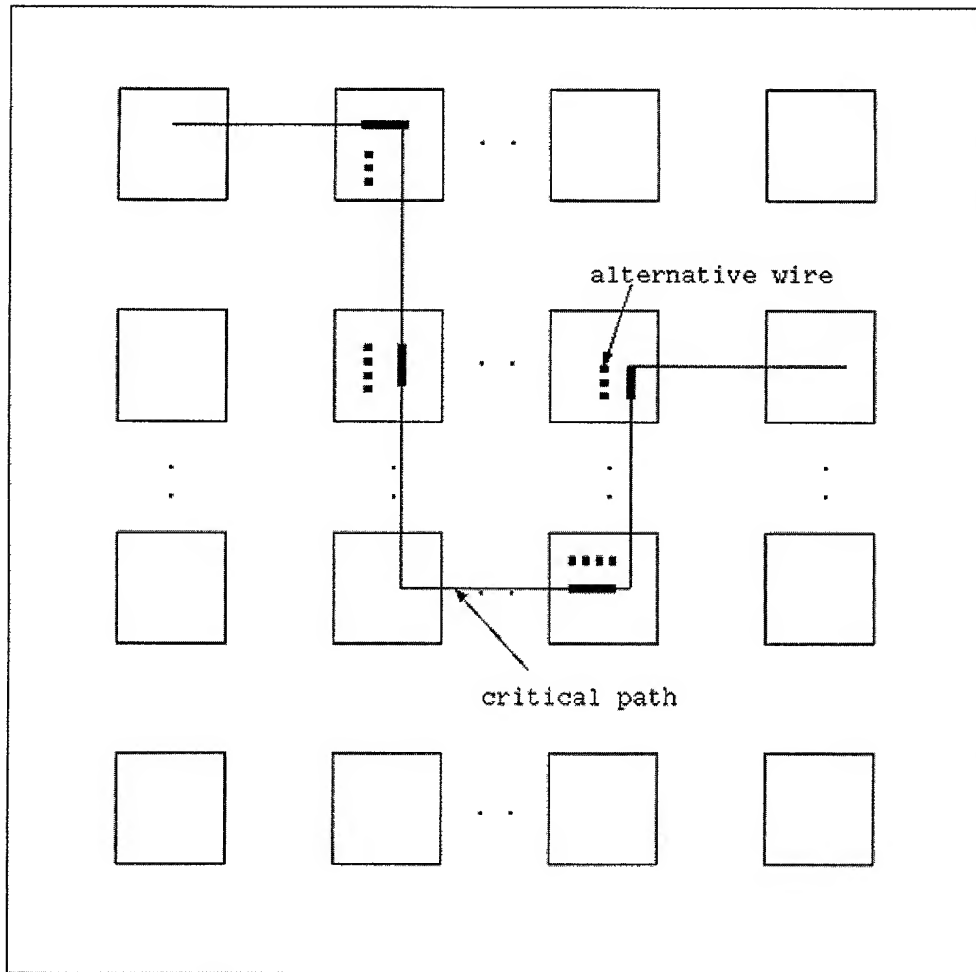


FIG. 8

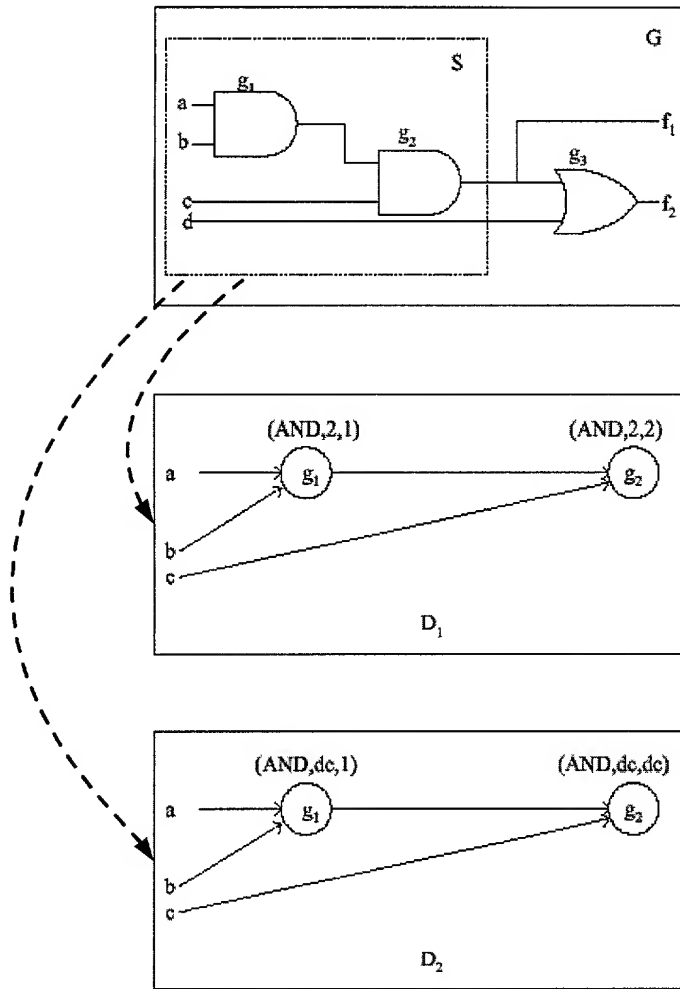


FIG. 9

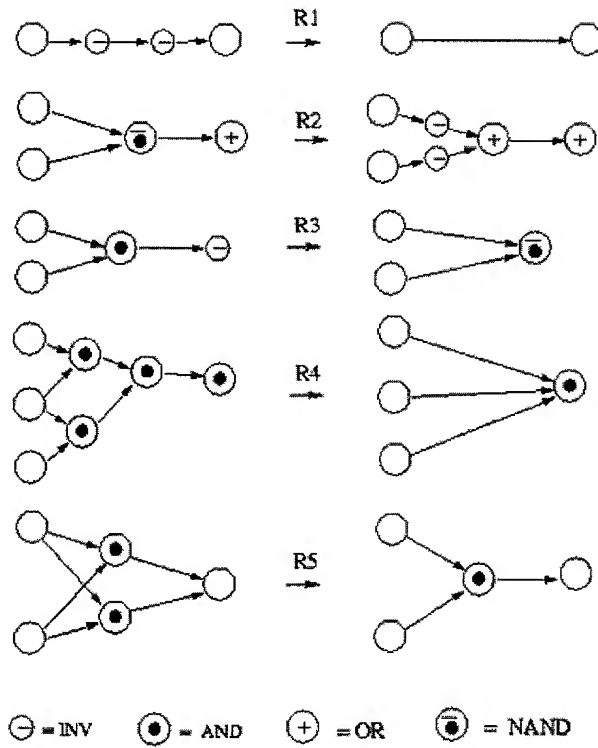


FIG. 10

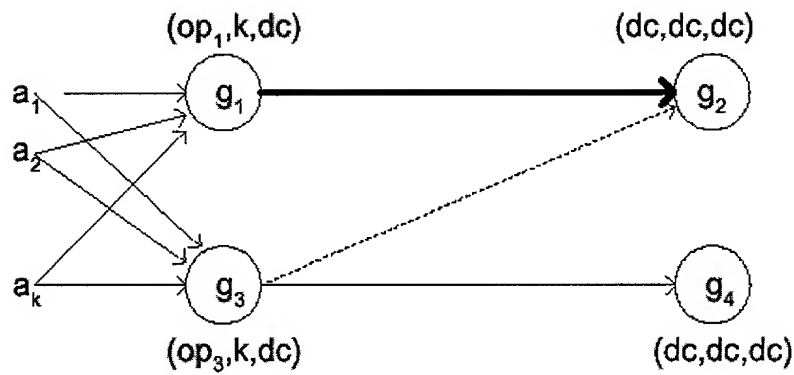
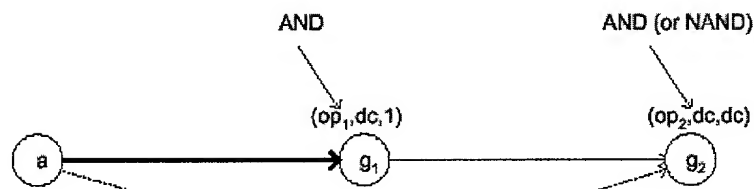
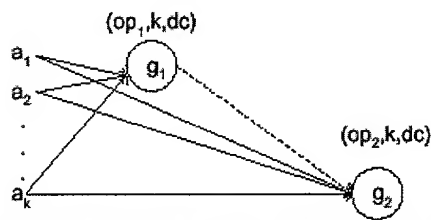


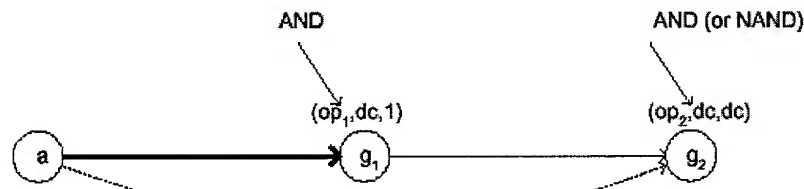
FIG. 11



(a) Case 1-1, $op_1=AND$, $op_2=AND$ (or NAND); or $op_1=OR$, $op_2=OR$ (or NOR)



(b) Case 1-2, $op_1=AND$, $op_2=AND$ (or NAND); or $op_1=OR$, $op_2=OR$ (or NOR)



(c) Case 1-3, $op_1=NOR$, $op_2=NAND$ (or AND); or $op_1=NAND$, $op_2=OR$ (or NOR)

FIG. 12

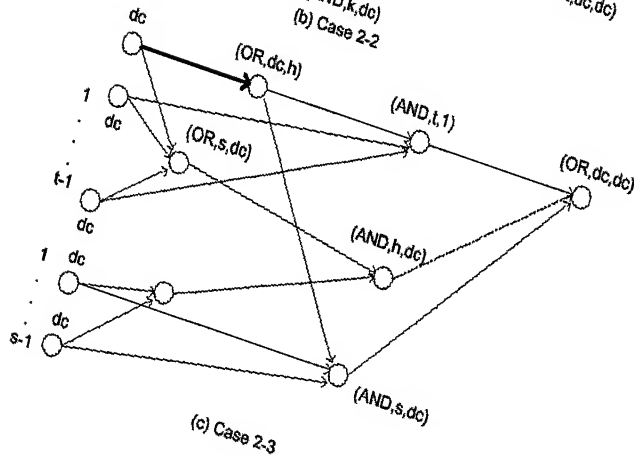
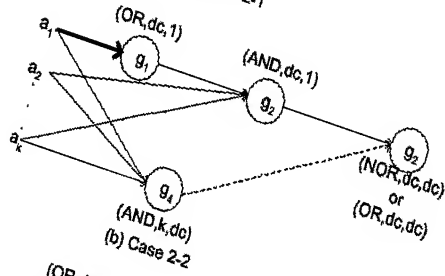
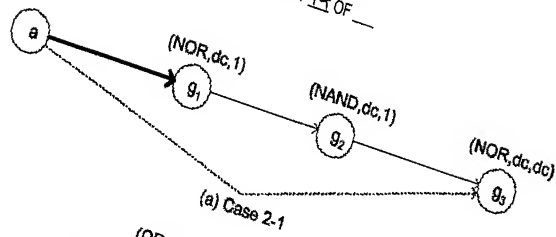


FIG. 13

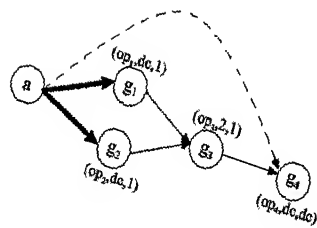
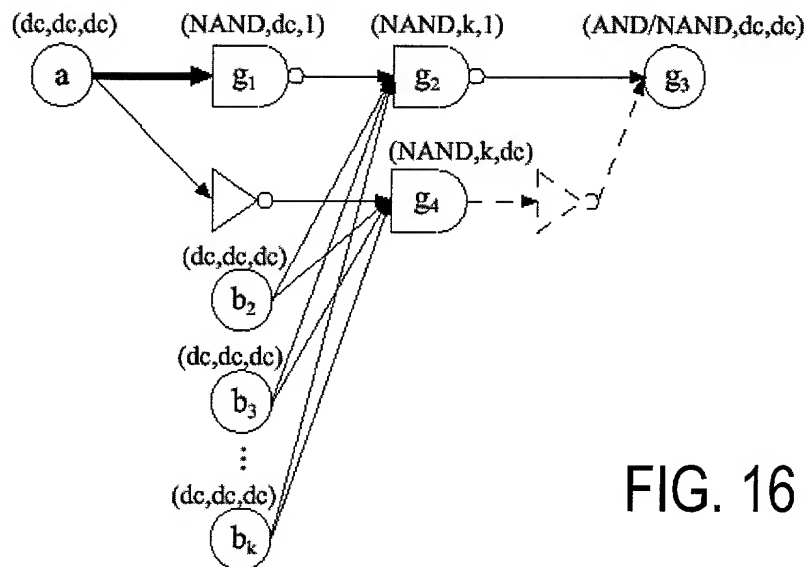
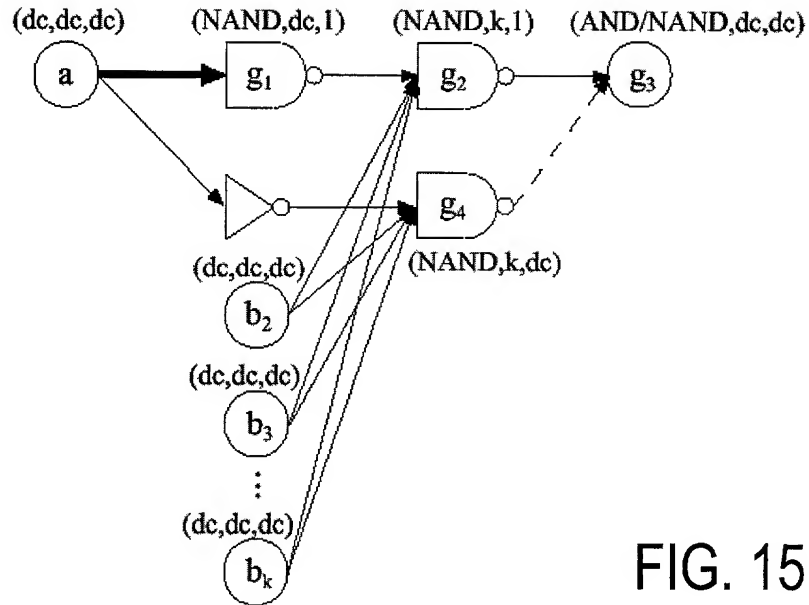


FIG. 14



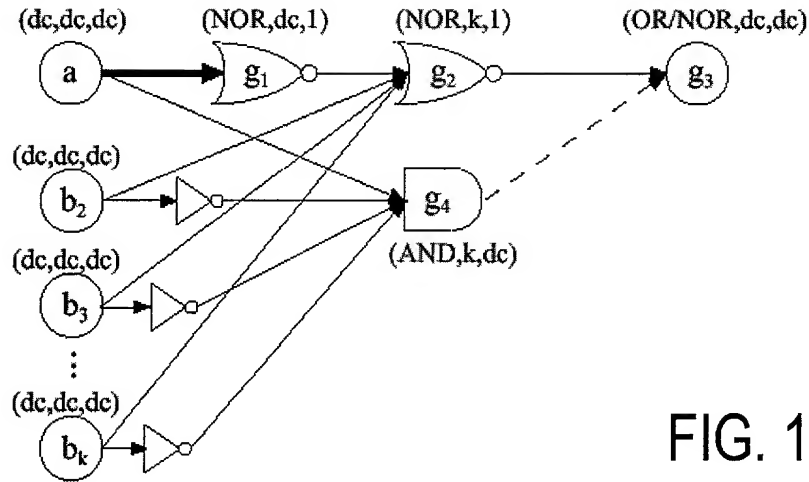


FIG. 17

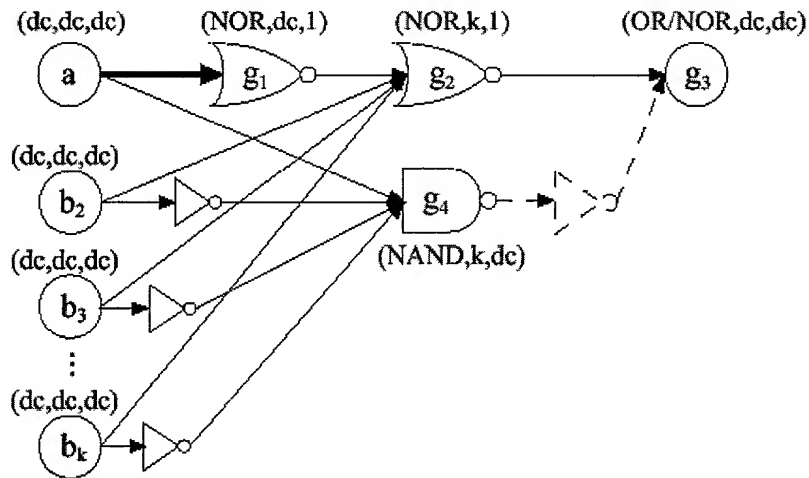


FIG. 18

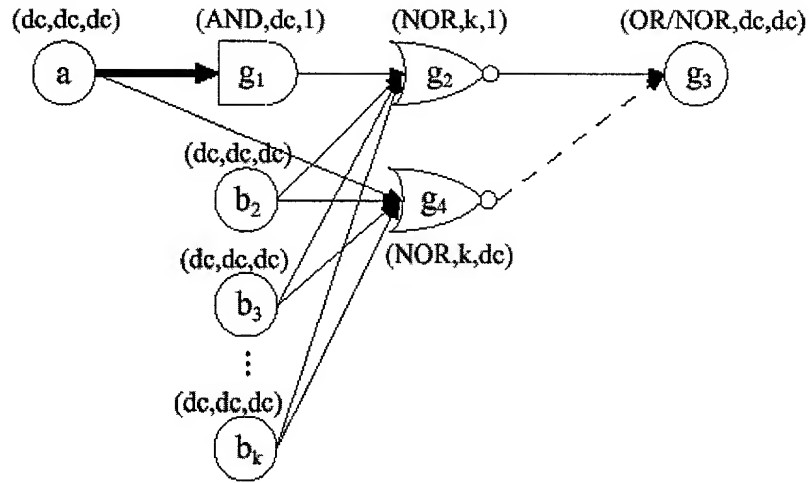


FIG. 19

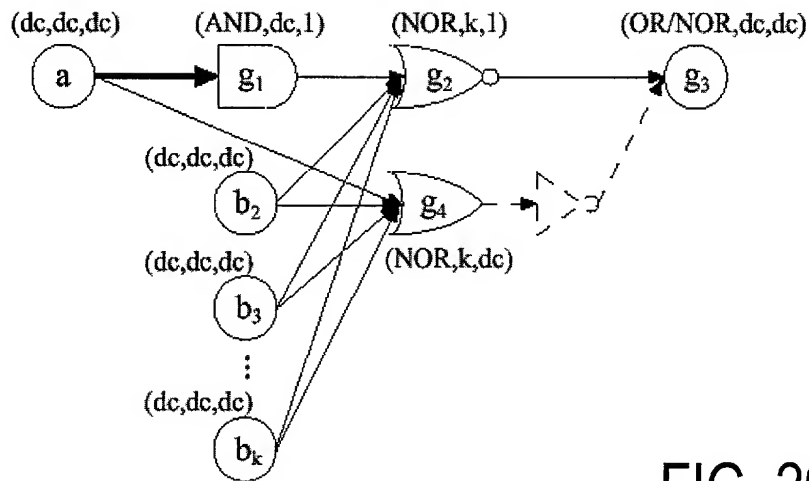
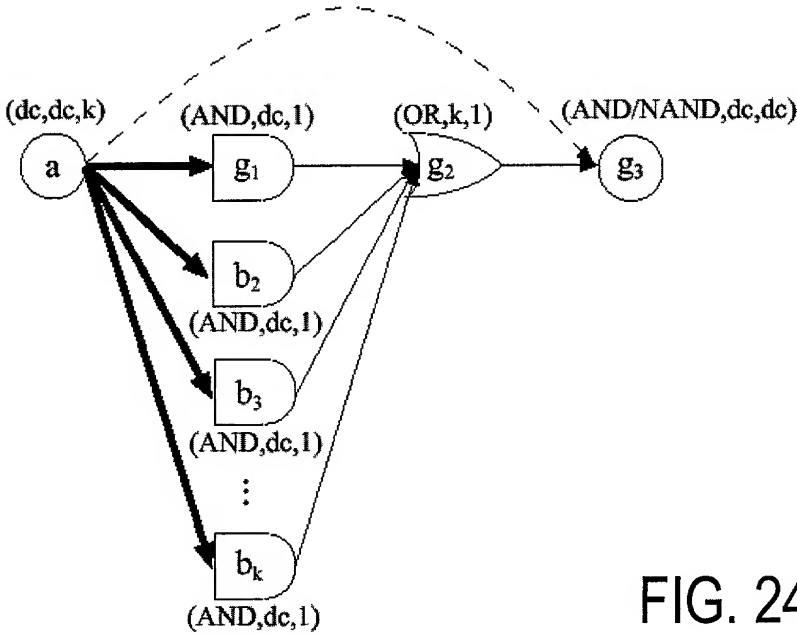
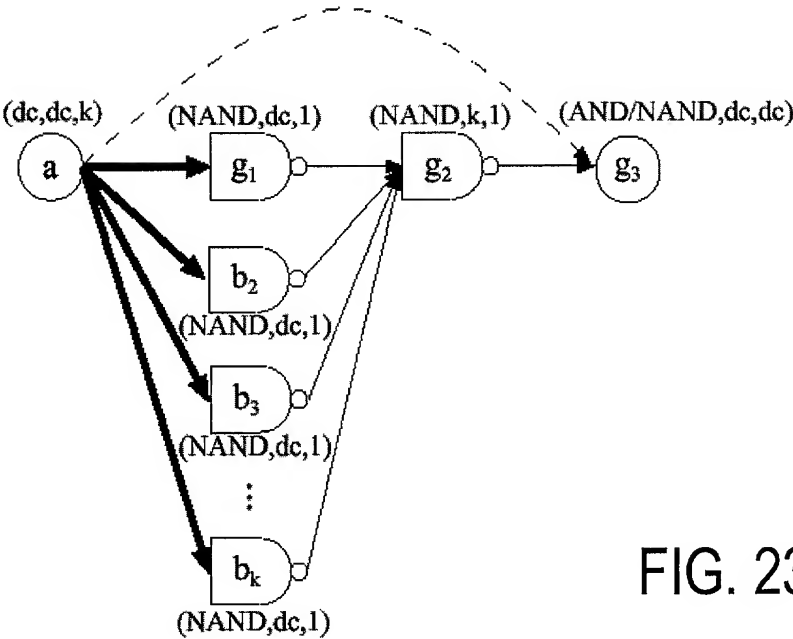


FIG. 20





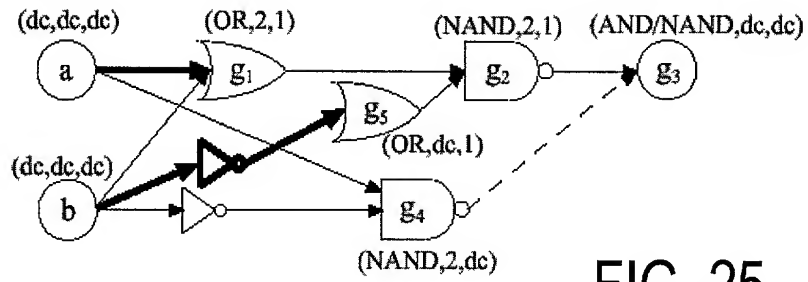


FIG. 25

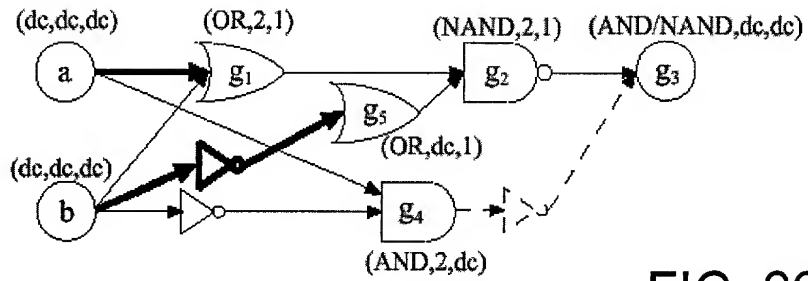


FIG. 26

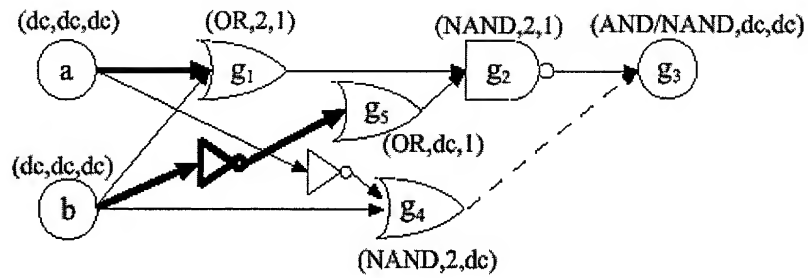


FIG. 27

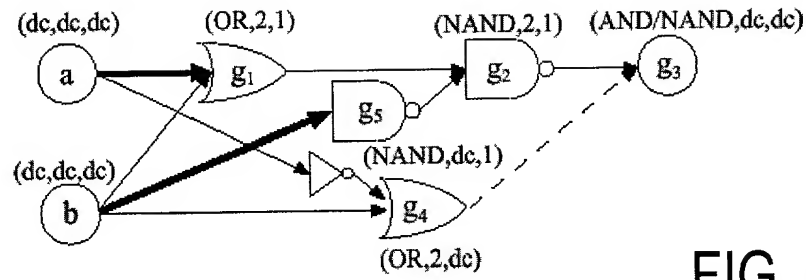


FIG. 28

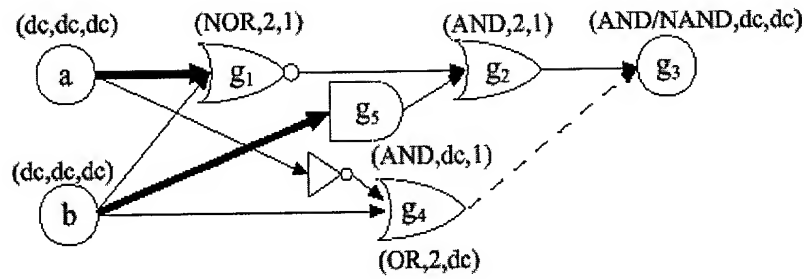


FIG. 29

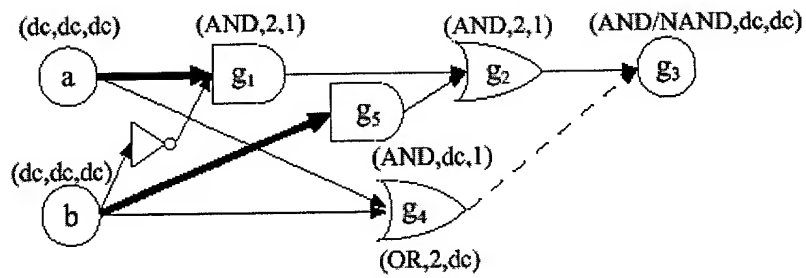


FIG. 30

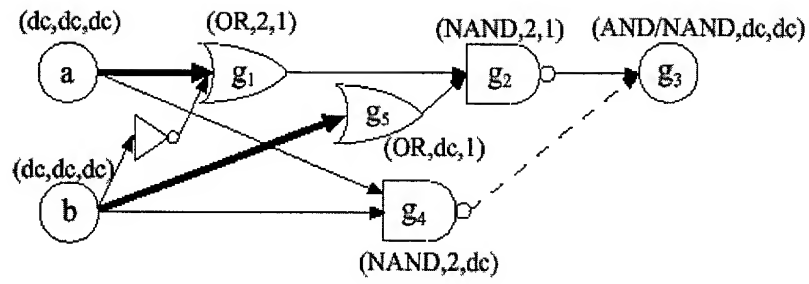


FIG. 31

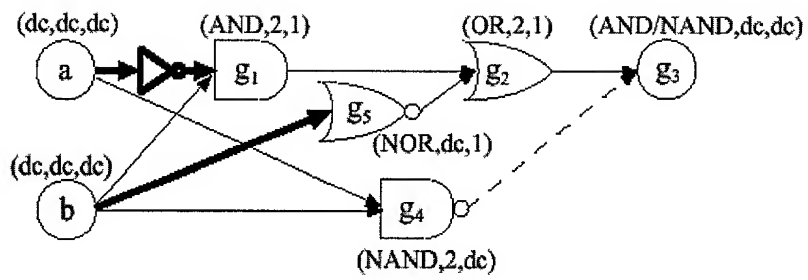


FIG. 32

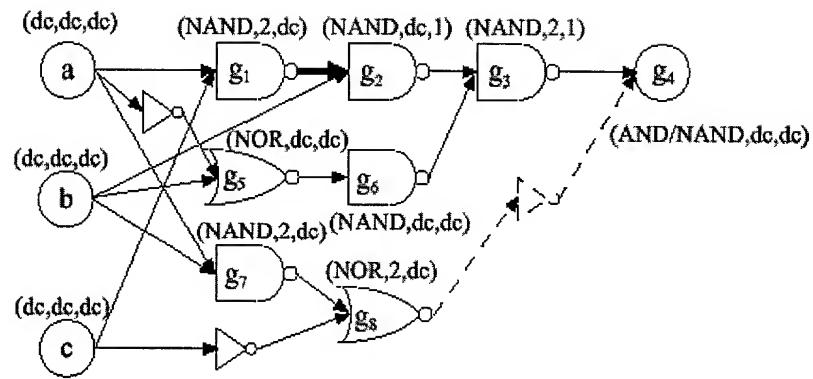


FIG. 33

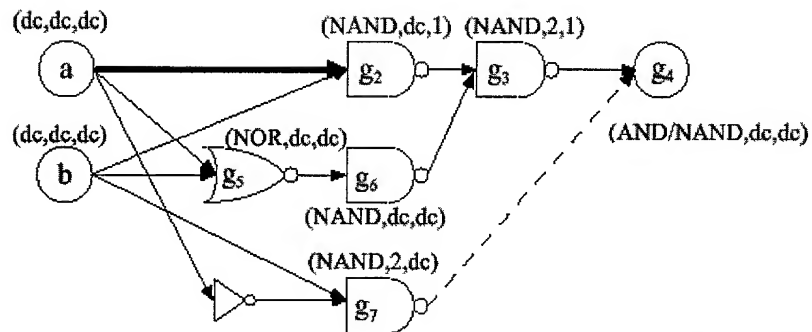


FIG. 34